A1

a second doped polysilicon layer over and in contact with the second undoped polysilicon layer, the second doped and undoped polysilicon layers forming a control gate.

A2

22. The memory cell of claim 17 wherein each of said first and second doped polysilicon layers are in-situ doped with impurities.

A3

26. A semiconductor transistor comprising:

an insulating layer over a substrate region;

an undoped polysilicon layer over and in contact with the insulating layer; and

a doped polysilicon layer over and in contact with the undoped polysilicon layer, the doped and undoped polysilicon layers forming a gate of the transistor, wherein the gate is electrically accessible.

A4

33. A semiconductor structure comprising:

an undoped polysilicon layer;

a doped polysilicon layer in contact with the undoped polysilicon layer; and

an insulating layer in contact with the undoped polysilicon layer, wherein the undoped polysilicon layer is sandwiched between the doped polysilicon layer and the insulating layer,

wherein the doped and undoped polysilicon layers form part of a gate which is electrically accessible.

REMARKS

Claims 1-35 are pending. Claims 1-16 are withdrawn from consideration. Claims 17 and 22 are amended to correct typographical errors. Claims 26 and 33 are amended to more clearly set forth the invention. Support for these claim amendments can be found throughout the specification and the drawings. No new matter is believed added.